SWITCH APPARATUS

Technical Field and Background of the Invention

The present invention refers the field of data and telecommunications, and more specifically to an apparatus in which a number of switch elements are combined into forming a larger scale switch.

When designing and operating communication networks and components, there are many situations in which scalability when it comes to switching capacity and flexibility is of great advantage. The option of handling smaller switch elements that, if necessary or desired, may be combined into forming larger switches with greater capacity allows greater design freedom and simplifies product logistics.

When for example using a 4×4 (4 input ports and 4 output ports) switch element as building block, an 8×8, as wll as a 16×16 or 32×32 switch can be built based thereupon. Thus, instead of designing, producing, and logistically handling and supporting four different swtch architectures, only one scaleable architecture would require such attention.

Similarly, scalability when operating products in larger networks has the advantage of lowering operating cost and simplifying design and operation as one product can be configured for use in many different situations having different switching requirements.

A disadvantage with prior art schemes for combining switch elements into forming lager scale switches is that they a) often require complex interconnecting and configuration schemes, b) require internal modification of the individual switch elements, or c) do not combine the individual switch element into a switch that offers non-blocking operation.

Summary of the Invention

An object of the invention is to provide a switch architecture in which a number of switch elements are combined into forming a larger scale switch and in which interconnections and configurations of the switch elements are simple, requires little or no internal configuration of the individual switch elements, and results in a switch that offers non-blocking operation.

This and other object are achieved by the invention as defined in the accompanying claims.

The invention is based upon the use of a switch element in which the relationship between an output port and each one of one or more input ports thereof is such that time-switching is performed, according to switch instructions provided by a control unit, with respect to one or more slots that are received at the respective input port and that are to be switched to the output port, and in which the relationship between said output port and an additional input port is such that no time-switching is performed with respect to slots that are received at said additional input port and that are switched to said output port.

Furthermore, the invention defines ways in which switch elements of this kind are to be interconnected to form larger scale switches, using said additional port as means for interconnecting the switch elements. Typically, said additional port is used to receive an input from another switch element, said input already having been at least time-switched by said another switch element.

According to a preferred embodiment, each switch element comprises, for each one of said one or more in put ports, a second additional output port, referred to as repeat port, wherein data received at the respective one of said one or more input ports is transmitted from the respective repeat port as received at the respective input port, thereby making it possible to provide an

input signal to several switch elements by connecting them in series using said repeat port.

According to another preferred embodiment, the switch elements of the invention are arranged to receive and transmit data in essentially equally sized, e.g. 125 µs, frames, said frame typically being divided into fixed size, e.g. 64-bit, time slots. Furthermore, the data transfer within and between the switch elements that form a larger scale switch according to the invention is also preferably performed in the context of frames of data. For example, the invention will be applicable for building switches in so-called DTM (Dynamic synchronous Transfer Mode) networks. For further information on such a network, reference is made to "The DTM Gigabit Network", Christer Bohm, Per Lindgren, Lars Ramfelt, and Peter Sjödin, Journal of High Speed Networks, 3(2):109-126, 1994.

To further exemplify and describe a preferred way in which time and, optionally, space switching is performed in said switch element with respect to said one or more input ports, reference is made to the not yet published Swedish Patent Application 9704067-9.

The above mentioned features, embodiments and aspects of the invention will now be further exemplified with reference to the accompanying drawing.

Brief Description of the Drawings

Exemplifying embodiment of the invention will now be described with reference to the accompanying drawings, wherein:

Fig. 1 schematically shows an embodiment of a switch element of the kind used to build larger scale switches according to the invention;

Fig. 2 schematically shows an example on the design of the time-switching circuit illustrated in Fig. 1;

Fig. 3 schematically shows an embodiment of a switch that is built up by interconnected switch elements of the kind shown in Fig. 1;

Fig. 4 schematically shows the switch of Fig. 3 according to a modified embodiment;

Fig. 5 schematically shows another embodiment of a switch element of the kind used to build larger scale switches according to the invention;

Fig. 6 schematically shows an embodiment of a switch that is built up by interconnected switch elements of the kind shown in Fig. 5;

Figs. 7A and 7B schematically shows sixteen 4x4 switch elements that are combined into forming a 16x16 switch.

Detailed Description of Preferred Embodiment

An exemplifying embodiment of a switch element of the kind used to build larger scale switches according to the invention will now be describe with reference to Fig. 1. In Fig. 1, the switch element 100 comprises a first input port 110, a second input port 120, a time-switching circuit 130, a selecting multiplexor 140, and an output port 150.

In operation, the first input port 110 will typically be connected to receive data in essentially fixed sized frames that are divided into fixed sized slots. For exemplifying purposes, it will throughout the drawings be assumed that the frame length is 125 μs and that each slot comprises 64 bits of data. The frames received via the input port 110 are forwarded to the time-switching circuit 130. The time-switching circuit 130 is arranged to provide for time-switching of the slots of each received frame, in accordance with time-switching instructions provided by a switching control unit (not shown), to provide an output frame of slots to the selecting multiplexor 140. An example on the design of the time-switching

circuit will be described more in detail below with reference to Fig. 2.

In parallel, the second input port 120 will optionally be connected to receive data in similar, essentially fixed sized frames. However, the frames of data that are received via the second input port 120 are forwarded directly to the selecting multiplexor 140, i.e. with the time sequential order of the slots of each frame maintained.

Consequently, if both input ports of the switch element 100 are connected to receive frames of data, the selecting multiplexor will simultaneously be provided with a) frames from the time-switching circuit 130, the slots of the frames having been time-switched as compared to their locations in the frames when received at the input port 110, and b) frames from the second input port, the time slots thereof not having been time-switched.

The selecting multiplexor 140 is arranged to output frames that are to be transmitted from the output port 150 of the switch element 100 by selectively, in accordance with switching instructions provided by the above-mentioned switching control unit, combining slots of frames received from the time-switching circuit 130 with slots of frames received directly from the second input port 120. In the exemplifying embodiment illustrated in Fig. 1, the selecting multiplexor 140 is arranged to select, for each slot forwarded to the output port 150, either a slot received from the time-switching circuit 130 or a slot received from the second input port 120. More specifically, as the n:th time slot of a frame that is currently forwarded to the output port 150, the selecting multiplexor 140 will select either the n:th slot of the frame that is currently received from the time-switching circuit 130 or the n:th slot of the frame that is currently received from the second input port 120. To be noted, if the second input port 120 is not connected to receive any input signal, the selecting

multiplexor will be instructed to simply forward the entire frames of slots as received from the time-switching circuit 130.

As will be illustrated more in detail below, when combining the switch element 100 with additional similar switch elements to build a larger scale switch, the first input port 110 will typically be connected to receive an input signal of the larger scale switch and the second input port 120 will be either not connected to receive any signal at all or connected to an output port of another switch element forming the larger scale switch. Consequently, an input port having a non time-switching function and being used to provide for connection to output ports of other switch elements of a larger scale switch, like the input port 120, will sometimes be referred to below as a cascade input port.

An example on the design of the time-switching circuit 130 shown in Fig. 1 will now be described with reference to Fig. 2.

In Fig. 2, the time-switching circuit 130 is arranged to perform time-switching with respect to slots of frames received as input 209 (from port 110 in Fig. 1) to provide output frames as output 231 (to port 150 in Fig. 1). The input frames 209 are provided to a demultiplexor 210. At the same time, a frame synchronization signal 208, which defines the start of each frame received as input 209, synchronizes the operation of an input slot counter 240 and a write buffer selecting unit 250. The write buffer selecting unit 250 is arranged to control the demultiplexor 210, at the rate of the frame synchronization signal, to have it forward each frame of the input 209 sequentially to one of three frame buffers 220a, 220b, and 220c of a frame memory 220 in a modulo-3 fashion. At the same time, the input slot counter 240 controls which entry of the buffer that each specific slot of the frame is written into. The input slot counter 240 is reset on each reception of the frame synchroniza-

tion signal 208 and counts, at the rate of a slot frequency, from a first entry to a last entry of the buffer in sequential order, the slots of each frame thereby being written into the frame buffer to be located therein with maintained sequential slot order.

On the output side, an output frame synchronization signal 232 is used to synchronize operation of an output slot counter 260 and a read buffer selecting unit 270. The output slot counter 260 is reset on each reception of the output frame synchronization signal 232 and counts, at the rate of a slot frequency, to address a first entry to a last entry of a slot mapping table 280 (which may be said to in part form the above-mentioned switching control unit) in sequential order, thus stepping through the slot mapping table once for each output frame. For each specific output slot, the output slot counter 260 will point at a respective entry of the slot mapping table 280. The slot mapping table 280 in turn provides, at each entry, a respective address to the frame memory 220, designating from which entry thereof that slot data is to be retrieved. The entries of the slot mapping table 280 thus define the desired time-switching of the input frame. At the same time, the read buffer selecting unit 270 controls, via the multiplexor 230, from which one of the three frame buffers 220a, 220b, and 220c that slot data is currently to be forwarded, stepping through the three buffers in a modulo-3 fashion at the rate of the output frame synchronization signal 232. As is understood, the function of the write and read buffer selection units 250 and 270 is to make sure that a stored frame is not overwritten until it has been properly read.

An exemplifying embodiment of a switch that is built up by interconnected switch elements of the kind described above with reference to Fig. 1 will now be described with reference to Fig. 3. In Fig. 3, the switch 300 is arranged to perform time and space switching from a first 310 and a second 320 input signal to a first 330 and a

second 340 output signal, all being assumed to be formed by fixed size frames that are divided into fixed size slots. For that purpose, the switch comprises four switch elements 100a-100d of the kind described above with reference to Fig. 1.

As is illustrated, the first input port 110a of the first switch element 100a and the first input port 110b of the second switch element 100b are connected to receive the first input signal 310. Similarly, the first input port 110c of the third switch element 100c and the first input port 110d of the fourth switch element 100d are connected to receive the second input signal 320.

To cascade the switch elements, the output port 150a of the first switch element 100a is connected to the second input port 120c of the third switch element 100c, and the output port 150b of the second switch element 100b is connected to the second input port 120d of the fourth switch element 100d. To be noted, as the first 100a and second 100b switch elements do not have and cascaded inputs, the second input ports 120a, 120b thereof are not connected to receive any input signals.

The first and second output signals 330 and 340 are thereby provided as the output from the output port 150c of the third switch element 100c and the output port 150d of the fourth switch element 100d.

In the switch 300 of Fig. 3, the time-switching circuit 130a of the first switch element 100a will be configured to perform all time-switching necessary with respect to slots of the first input signal 310 that are to be transmitted in frames of the first output signal 330. Similarly, the time-switching circuit 130b of the second switch element 100b will be configured to perform all time-switching necessary with respect to slots of the first input signal 310 that are to be transmitted in frames of the second output signal 340. The so time-switched frames of the first input signal 310 are then forwarded to the selecting multiplexors 140c and 140d of

the third and fourth switch element 100c and 100d, respectively using the cascade input ports 120c and 120d.

In addition, the time-switching circuit 130c of the third switch element 100c will be configured to perform all time-switching necessary with respect to slots of the second input signal 320 that are to be transmitted in frames of the first output signal 330, and the time-switching circuit 130d of the fourth switch element 100d will be configured to perform all time-switching necessary with respect to slots of the second input signal 320 that are to be transmitted in frames of the second output signal 340. The so time-switched frames of the second input signal 320 are thus also forwarded to the selecting multiplexors 140c and 140d of the third and fourth switch element 100c and 100d, respectively.

The selecting multiplexor 140c will then form the first output signal 330 by selecting slots from the first input signal 310 as received via the time-switching circuit 130a and the second input signal 320 as received via the time-switching circuit 130c. Similarly, the selecting multiplexor 140d will form the second output signal 340 by selecting slots from the first input signal 310 as received via the time-switching circuit 130b and the second input signal 320 as received via the time-switching circuit 130d.

An alternative embodiment of a switch that is built up by interconnected switch elements of the kind described above with reference to Fig. 1 is shown in Fig. 4. In the switch 400 of Fig. 4, each switch element 100a-100d is provided with a respective so-called repeat port 125a-125d. The repeat port of a switch element has the function of simply forwarding any data that is received via the first input port of the respective element. Then, instead of connecting an input signal (such as the input signal 310 in Fig. 3) directly to first input ports of two different switch element (such as 100a and 100b in Fig. 3), the input signal is only connected to the input

port of one of these two elements, the other one of the two elements simply being provided with the input signal by having its first input port connected to the repeat port of the first element.

For example, in Fig 4, the first input port 110b of the second switch element 100b receives the first input signal 310 by being connected to the repeat port 125a of the first switch element 100a, and the first input port 110d of the fourth switch element 100d receives the second input signal 320 by being connected to the repeat port 125c of the third switch element 100c. To be noted, as the input signals 310 and 320 are in this example not to be forwarded to any switch elements in addition to the ones shown in the figure, the repeat ports of the second 100b and fourth 110d switch elements are in this case not connected to forward any signals to other switch elements. With the exemption of this use of the repeat ports, the design and operation of the switch 400 of Fig. 4 is the same as the design and operation of the switch 300 of Fig. 3.

Another exemplifying embodiment of a switch element of the kind used to build larger scale switches according to the invention will now be describe with reference to Fig. 5. In Fig. 5, the switch element 500 comprises a first 510, a second 520, a third 511, and a fourth 521 input port, a first 530 and a second 531 time-and-space-switching circuit, a first 540 and a second 541 selecting multiplexor, and a first 550 and a second 551 output port.

The first switching circuit 530 is arranged to provide for time-and-space-switching of slots of frames received via the first input port, in accordance with time-and-space-switching instructions provided by a switching control unit (not shown), to provide an output frame of slots to the first multiplexor 540, and an output frame of slots to the second multiplexor 541. Similarly, the second switching circuit 531 is arranged

to provide for time-and-space switching of slots of frames received via the third input port 511, in accordance with time-and-space-switching instructions provided by a switching control unit (not shown), to also provide an output frame of slots to the first multiplexor 540, and an output frame of slots to the second multiplexor 541. As understood, the design and operation of each one of the time-and-space-switching circuits 530, 531 may be similar to the circuit described above with reference to Fig. 2. For example, the frame memory illustrated in Fig. 2 could simply be provided with an additional read port, output multiplexor and slot selecting mechanism to provide the desired additional output signal.

In parallel, the second 520 and the fourth 521 input port will optionally be connected to forward frames as received directly to the multiplexor 540 and 541, respectively, i.e. with the time sequential order of the slots of each frame maintained.

Each one of the selecting circuits 540, 541 is then arranged to output frames that are to be transmitted from the respective output port 550, 551 by selectively, in accordance with switching instructions provided by a switching control unit (not shown), combining the slots of frames received a) from the circuit 530, b) from the circuit 531, and c) directly from the respective cascade input port 520, 521. For example, in the exemplifying embodiment illustrated in Fig. 5, the selecting circuit 540 is arranged to forward, as the n:th time slot of a frame that is currently forwarded to the output port 550, either the n:th slot of the frame that is currently received from the circuit 530, the n:th slot of the frame that is currently received from the circuit 531, or the n:th slot of the frame that is currently received directly from the input port 520.

An exemplifying embodiment of a switch that is built up by interconnected switch elements of the kind described above with reference to Fig. 5 will now be

described with reference to Fig. 6. In Fig. 6, the switch 600 is arranged to perform time and space switching from frames of four input signals 610-640 to frames of four output signals 650-680 and comprises said four switch elements 500a-500d of the kind described with reference to Fig. 5.

As shown in Fig. 6, the first input port of the first element 500a and the first input port of the second element 500b are connected to receive the first input signal 610, the third input port of the first element 500a and the third input port of the second element 500b are connected to receive the second input signal 620, the first input port of the third element 500c and the first input port of the fourth element 500d are connected to receive the third input signal 630, and the third input port of the third element 500a and the third input port of the fourth element 500d are connected to receive the fourth input signal 640.

To cascade the elements 500a-500c into forming the larger scale switch 600, the first and second output port of the first element 500a is connected to the second and fourth input port, respectively, of the third element 500c, and the first and second output port of the second element 500b is connected to the second and fourth input port, respectively, of the fourth element 500d.

The first 650, second 660, third 670 and fourth 680 output signal is thereby provided as the output from the first output port of the third element 500c, the second output port of the third element 500c, the first output port of the fourth element 500d, and the second output port of the fourth switch element 500d, respectively.

To exemplify the configuration of the switching and multiplexing circuits of the elements 500a-500c when switching time slot from frames of the four input signals 610-640 to, for example, the first output signal 650, the first time-and-space-switching circuit of the first switch element 500a will be configured to perform all

time-switching necessary, with respect to slots of the first input signal 610 that are to be transmitted in frames of the first output signal 650, when providing its output to the first multiplexor of the first switch element 500a. Similarly, the second time-and-space-switching circuit of the first switch element 500a will be configured to perform all time-switching necessary, with respect to slots of the second input signal 620 that are to be transmitted in frames of the first output signal 650, when providing its output to the first multiplexor of the first switch element 500a. The first multiplexor of the first switch element 500a will in turn be configured perform all space selection necessary, with respect to slots of the first 610 and the second 620 input signal that are to be transmitted in frames of the first output signal 650, when providing its output to the first cascade input of the third switch element 500c.

In the switch element 500c, the first time-and-space-switching circuit thereof will be configured to perform all time-switching necessary, with respect to slots of the third input signal 630 that are to be transmitted in frames of the first output signal 650, when providing its output to the first multiplexor. Similarly, the second time-and-space-switching circuit of the third switch element 500c will be configured to perform all time-switching necessary, with respect to slots of the fourth input signal 640 that are to be transmitted in frames of the first output signal 650, when providing its output to the first multiplexor of the third switch element 500c. Finally, the first multiplexor of the third switch element 500a will be configured to perform all space selection necessary among frames received from the first switching circuit (referring to input signal 630), the second switching circuit (referring to input signal 640), and the clustered input port (referring to input signals 610 and 620) to provide the desired output signal 650.

To further illustrate the cascading possibilities provided by the invention, Fig. 7A illustrate a 4x4 switch element, sixteen of which having been combined in Fig. 7B into forming a 16x16 switch.

As is shown in Fig. 6A, the switch element has four signal inputs, four signal outputs, four cascade inputs and four repeat outputs. The design and operation of this switch element could for example be similar to the design and operation of the element 500 described above with reference to Fig. 5 by merely adding thereto two additional input port pairs, two switching circuits, two multiplexors, and two output ports, and by providing each one of the then four switching circuits of the element with the capability of providing frames of time switched slots to all four multiplexors of the element, each multiplexor thus selecting time slots among frames provided by the four switching circuits and a respective one of the cascade input ports.

To be understood, even though the invention primarily addresses so-called symmetric or quadratic switch element configurations, for example as illustrated in Figs 3, 7, and 7B, also asymmetric switch element configurations can be envisaged.

Even though exemplifying embodiment of the invention has been described in detail above, modifications, combinations and alterations thereof may be made, as will be clear to those skilled in the art, within the scope of the invention, which is defined by the accompanying claims.